Band-to-band tunneling devices from two-dimensional materials

Abhijith Prakash*, Peng Wu*, and Joerg Appenzeller
Electrical and Computer Engineering, Purdue University, West Lafayette, Indiana 47907
appenzeller@purdue.edu, *phone: 765-494-1076*

Band-to-band (BTB) tunneling devices have been proposed as an alternative to conventional MOSFETs more than a decade ago and have been demonstrated to achieve inverse subthreshold slopes (SS) below the thermal limit of around 60mV/dec at room temperature, making them a promising device concept for low-power applications [1,2]. In an ideal BTB tunneling field-effect transistor (TFET) an n/i/p or p/i/n doping profile is used, where the intrinsic portion of the channel is under gate control. By moving the conduction and valence bands of the i-region relative to the p- and n-regions, band-to-band tunneling is enabled with a tunneling window that is defined by the band edges of the p-to-i (or n-to-i) segments of the device.

In this work, we report the experimental demonstration of black phosphorus (BP) BTB TFETs with such a doping profile (p/i/n) and discuss the performance of these devices in the context of their on-state currents, an important metric that has concerned many researchers for years. Moreover, we evaluate the impact of channel body thickness and gate dielectric film thickness for both BP and WSe_2 BTB TFETs, showing the potential of aggressively scaled tunneling devices to achieve on-currents well above 100μA/μm at a V_{DD} of 0.2V and in excess of 1000μA/μm at V_{DD}=0.5V.

Devices were fabricated by defining source/drain metal electrodes from Ti/Au (10nm/20nm) on a Si/SiO_2 substrate. Subsequently, BP was mechanically exfoliated onto the contacts and a 0.8nm HfO_2 plus 1.5nm Al_2O_3 ALD layer was deposited to form the gate dielectrics in the G1 and G2 regions (see figure 1). Next, the gates G1 and G2 were defined by e-beam lithography and Ti (40nm) deposition. To achieve proper isolation between gates G1/G2 and G while not obtaining a "too thick" gate dielectric layer underneath G, etching of the Al_2O_3 layer was performed in the region between G1 and G2, and then a new 5nm thick Al_2O_3 layer was deposited to form the gate dielectric for gate G. The device is finished by depositing Cr/Au (5nm/15nm) to form the gate G. Figure 1a) shows a top view scanning electron microscopy (SEM) image of a readily fabricated triple gate BP TFET. With the full control over the three gated regions in the device, I_D vs. V_G was scanned as a function of V_{G1}. This approach allows to unambiguously identify whether BTB tunneling actually occurs. Figure 2 shows in this context, the evolution from an n-type MOSFET to an n-TFET. Note that when all gates are positive conventional MOSFET operation is obtained, while applying a progressively more negative voltage to gate G1 first suppresses electron transport from source to drain (see green measurement range) and ultimately results in the current increasing again when BTB tunneling conditions are satisfied (red curves) for high negative V_{G1} values and positive V_G values. The observed non-monotonic trend is clear evidence for our claim of BTB tunneling in BP as reported here. BTB tunneling on-current levels achieved in this device at V_{ds}=0.5V are in the 100nA/μm range for a BP body thickness of 10nm and a gate dielectric film thickness of around 4nm across the entire channel. To use these experimental insights to make proper projections about the performance of BTB TFETs, simulations following the discussions in references [3,4] were performed to calculate iso on-current lines as a function of materials parameters m* and E_g as well as the effective tunneling distance $\Lambda = 2 \cdot \sqrt{\frac{\varepsilon_{body}}{\varepsilon_{ox}} t_{body} t_{ox}}$. Figure 3 summarizes the simulation results and presents our experimental data at the same time. With Λ~13nm in our experiment and a value of $\sqrt{m^* E_g} \sim 0.163 \sqrt{m_0 eV}$, the experimentally determined on-currents as marked by the "red stars" are nicely in line with the expected trend for the "red" triangular simulations, when extrapolating to thicker channels. This fact supports that the simulations shown in figure 3 can be used to make quantitative predictions about the on-state performance of BP channels with different body thicknesses and devices with scaled gate dielectrics as well as other materials. Figure 3 a) and b) display the expected on-current levels for WSe_2 and BP BTB TFETs as a function of layer number (i.e. body thickness) for three different EOT values. Note that changing the body thickness has an immediate impact in particular on the bandgap and the dielectric constant of the channel material as well as the tunneling distance Λ. To create this plot, experimentally observed data on the change of E_g with body thickness from references [5] and [6] were used. Figure 3 clearly shows that ultra-thin body thicknesses in combination with scaled gate dielectrics allow readily achieving on-currents in BTB TFETs in the 100μA/μm to 1000μA/μm range. Last, it is worth noting that the observed SS values for the BP TFET (see figure 2) are consistent with the 10nm body thickness of the device according to our simulations and are expected to be reduced substantially by using thinner BP channels.

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** both authors contributed equally*

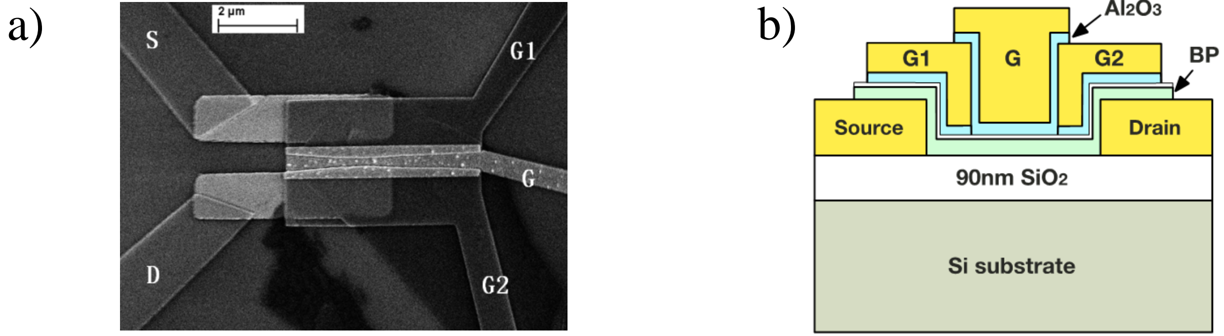

Figure 1: a) Scanning Electron Micrograph (SEM) of a readily fabricated black phosphorus (BP) band-to-band (BTB) tunneling transistor with three top gates allowing to create an p/i/n doping profile across the channel. b) Schematic illustration of the cross sectional view of the device in a). Note that the BP layer is located above the source drain contacts.

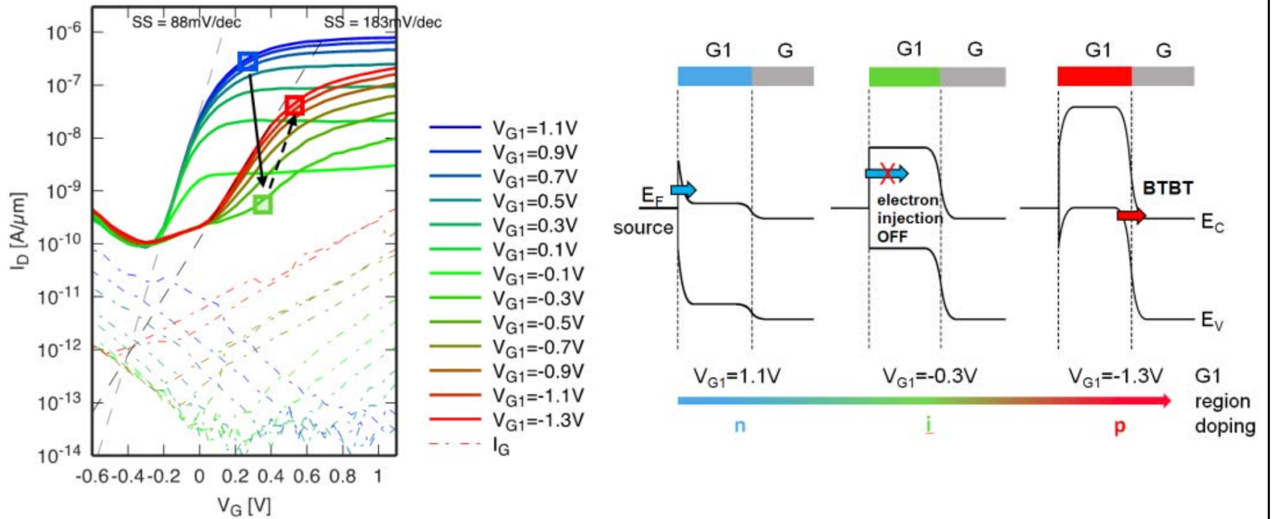

Figure 2: Experimental characteristics of the device from figure 1 with a body thickness of 10nm at V_{ds}=0.5V and V_{G2}=0.5V showing the transition from an n-type MOSFET to an n-type BTB TFET. The right side diagrams show how electrostatically doping the device in the G1-region from “n” to “p” opens the BTB tunneling window.

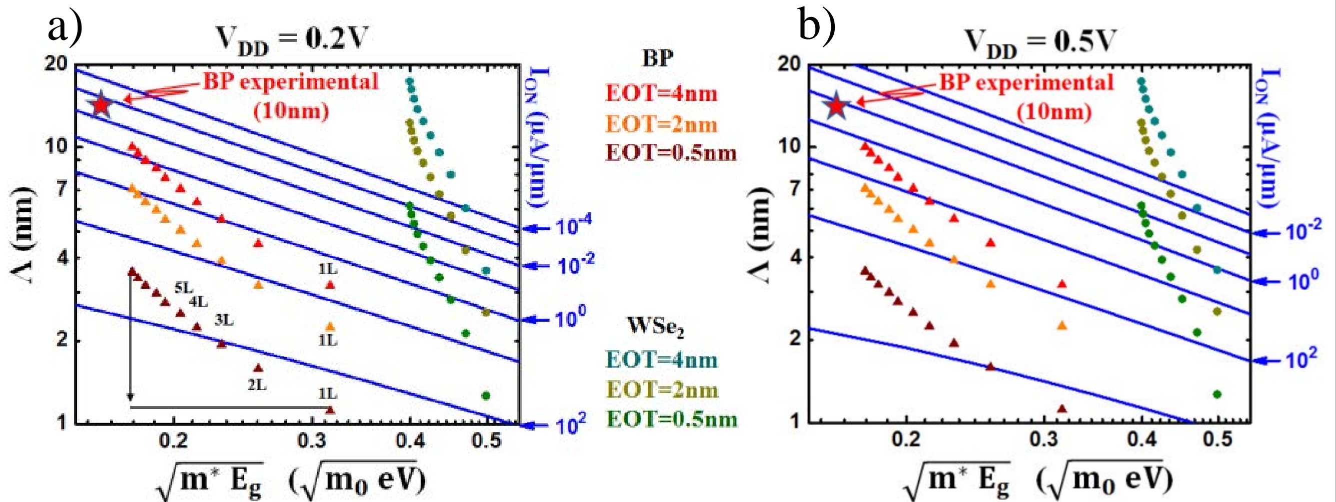

Figure 3: a) Calculated on-current levels of BP and WSe_2 TFETs at V_{DD}=0.2V. Different colors refer to different gate dielectric film thicknesses, and one group of symbols denotes the impact of body thickness (1L = one monolayer etc.) that results in a change of band gap and simultaneously in a change in the tunneling distance. b) Calculated on-current levels of BP and WSe_2 TFETs at V_{DD}=0.5V. Note that the “red stars” are experimentally obtained data (see figure 2) for a 10nm thick BP TFET.