

**“Multi-scale modeling of dielectric charging in RF-MEMS devices”**



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*Friday, Oct. 5<sup>th</sup>, 2012  
12:00 pm, Birck 2001*

**Abstract:** We present a multi-scale modeling approach to rigorously calculate the electron trap energy levels and accurately model the dielectric charging phenomenon in a-Si<sub>3</sub>N<sub>4</sub> dielectric, widely used for RF-MEMS devices. First principles charge state calculations are performed on an ensemble of a-Si<sub>3</sub>N<sub>4</sub> structures to quantify the location of trap levels in the energy band gap. We find that the electron traps lie across a range of energy levels, which are in excellent agreement with recent Trap Spectroscopy by Charge Injection and Sensing experiments on a-Si<sub>3</sub>N<sub>4</sub>. The calculations also provide valuable information about the microscopic nature of defects and their corresponding relaxation mechanisms caused by charge trapping. In addition to the commonly postulated III-Si defects (K centers), new defect mechanisms responsible for electron trapping have been identified. A comprehensive dielectric charging model to compute charge accumulation and leakage currents in an amorphous dielectric like a-Si<sub>3</sub>N<sub>4</sub> has been developed. We fit current transient measurements performed on MIM capacitors, and show that by using a distribution of trap levels from ab-initio calculations we are able to capture voltage and temperature dependences more accurately compared to using a single defect level, in spite of a reduction in empiricism. We observe an improvement of about 66% in relative error by using ab-initio informed dielectric charging simulations. From these calculations, we demonstrate that realistic modeling of the devices requires the incorporation of new multi-scale, multi-resolution approach spanning across various spatial and temporal scales.

**Speaker Bios:**

Ravi Vedula received his B.E. degree in Electronics and Communication Engineering from Osmania University, Hyderabad, India. He is currently pursuing a PhD degree in the school of Electrical and Computer Engineering at Purdue University. His research focuses on predictive atomistic modeling of electronic properties in realistic nanoscale devices.

Sambit Palit received his B.Tech. degree in electrical engineering and the M.Tech. degree in microelectronics from the Indian Institute of Technology Bombay, Mumbai, India in 2008. He is currently working towards a doctorate degree at Purdue University, West Lafayette, IN. His current research interests include reliability modeling and electrical characterization of thin-film dielectric-based devices, and, more broadly, in modeling and simulation of micro- and nano- electronic devices.